REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I. Editorial changes throughout.	90 JUN 28	W. Heckman
B	Changes to table I and switching waveforms. Editorial changes throughout.	92 MAY 14	T. Noh

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	A	B						
	SHEET	1	2	3	4	5	6	7	8	9	10	11						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Jeffery Tunstall

CHECKED BY
Tim H. Noh

APPROVED BY
W. HECKMAN

DRAWING APPROVAL DATE
9 NOVEMBER 1987

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, CLOCK GENERATOR AND READY INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87734

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87734	01	V	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	82C284-10	Clock generator and ready interface	10 MHz
02	82C284-8	Clock generator and ready interface	8 MHz
03	82C284-6	Clock generator and ready interface	6 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
All output and supply voltages	-0.5 V dc to +7 V dc
All input voltages	-1.0 V dc to +5.5 V dc
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case V	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage (V_{CC})	5 V dc ±5 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input high voltage	V_{IH}		1,2,3	All	2.0		V
$\overline{RES}$ and EFI input high voltage	V_{IHR}		1,2,3	All	2.6		V
RESET, PCLK output low voltage	V_{OL}	I_{OL} = 5 mA 2/	1,2,3	All		0.45	V
RESET, PCLK output high voltage	V_{OH}	I_{OH} = -1 mA	1,2,3	All	2.4		V
$\overline{READY}$, output low voltage	V_{OLR}	I_{OL} = 9 mA	1,2,3	All		0.45	V
CLK output low voltage	V_{OLC}	I_{OL} = 5 mA	1,2,3	All		0.45	V
CLK output high voltage	V_{OHC}	I_{OH} = -800 µA	1,2,3	All	4.0		V
Input leakage current	I_{LI}	$0\ V \le V_{IN} \le V_{CC}$ 3/	1,2,3	All	-10	+10	µA
Input sustaining current on S0, S1 pins	I_{IL}	V_{IN} = 0 V	1,2,3	All	-30	-500	µA
Power supply current	I_{CC}	At 20 MHz output CLK frequency	1,2,3	All		75	mA
Input capacitance	C_{IN}	F_C = 1 MHz, see 4.3.1c	4	All		10	pF
Functional tests		See 4.3.1d, V_{CC} = 4.75 V, 5.25 V	7,8	All			
EFI to CLK delay	t_1	At 1.5 V 4/	9,10,11	01		25	ns
				02		30	ns
				03		35	ns
EFI low time	t_2	At 1.5 V 4/ 5/	9,10,11	01	22.5		ns
				02	28		ns
				03	40		ns
EFI high time	t_3	At 1.5 V 4/ 5/	9,10,11	01	22.5		ns
				02	28		ns
				03	35		ns
CLK period	t_4		9,10,11	01	50	500	ns
				02	62	500	ns
				03	83	500	ns
CLK low time	t_5	At 1.0 V 2/ 4/ 6/ 7/	9,10,11	01	12		ns
				02	15		ns
				03	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLK high time	t_6	At 3.6 V 2/ 4/ 6/ 7/	9,10,11	01	16		ns
				02,03	25		ns
CLK rise time	t_7	1.0 V to 3.6 V 2/ 4/	9,10,11	01		8	ns
				02,03		10	ns
CLK fall time	t_8	3.6 V to 1.0 V 2/ 4/	9,10,11	01		8	ns
				02,03		10	ns
Status setup time	t_9	4/	9,10,11	01	20		ns
				02	22		ns
				03	28		ns
Status hold time	t_{10}	4/	9,10,11	All	1		ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ setup time	t_{11}	4/	9,10,11	01	17.5		ns
				02	20		ns
				03	25		ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ hold time	t_{12}	4/	9,10,11	01	2		ns
				02,03	0		ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ setup time	t_{13}	4/ 8/	9,10,11	01,02	0		ns
				03	5		ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ hold time	t_{14}	4/ 8/	9,10,11	All	30		ns
$\overline{RES}$ setup time	t_{15}	4/ 8/	9,10,11	01,02	20		ns
				03	25		ns
$\overline{RES}$ hold time	t_{16}	4/ 8/	9,10,11	All	10		ns
$\overline{READY}$ inactive delay	t_{17}	At 0.8 V 9/	9,10,11	All	0		ns
$\overline{READY}$ active delay	t_{18}	At 0.8 V 9/	9,10,11	01,02	0	24	ns
				03	0	33	ns
PCLK delay	t_{19}	2/ 10/	9,10,11	01	0	35	ns
				02,03	0	45	ns
Reset delay	t_{20}	2/ 10/	9,10,11	01	5	27	ns
				02	5	34	ns
				03	5	50	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
PCLK low time	t_{21}	10/ 11/	9,10,11	All	t_4-20		ns
PCLK high time	t_{22}	10/ 11/	9,10,11	All	t_4-20		ns

1/ See figures 3 and 4.

2/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

3/ Status lines $\overline{S0}$ and $\overline{S1}$ excluded because they have internal pull-up resistors.

4/ CLK loading: C_L = 100 pF.

5/ When driving with EFI, provide minimum EFI high and low times as follows:

CLK output frequency:	12 MHz	16 MHz	20 MHz
Min. required EFI high time	35 ns	28 ns	22.5 ns
Min. required EFI low time	40 ns	28 ns	22.5 ns

6/ With the internal crystal oscillator using recommended crystal and capacitive loading, or with the EFI input meeting specifications t_2 and t_3 use a parallel-resonant, fundamental mode crystal. The recommended crystal loading for CLK frequencies of 8-16 MHz are 25 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V_{CC} and GND as close to the device as possible.

7/ When using crystal (with recommended capacitive loading per table below) appropriate for speed of the device, CLK output high and low times guaranteed to meet 5962-85148 requirements.

Crystal frequency	C1 capacitance (pin 7)	C2 capacitance (pin 8)
1 to 8 MHz	60 pF	40 pF
8 to 20 MHz	25 pF	15 pF

Note: Capacitance values must include stray board capacitance.

8/ This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

9/ $\overline{READY}$ loading: I_{OL} = 9 mA, C_L = 150 pF. In system application, use 700Ω ±5 percent pull-up resistor to meet 5962-8514803 timing requirements and use 910Ω ±5 percent pull-up resistor to meet 5962-8514801 and 5962-8514802 timing requirements.

10/ PCLK and RESET loading: C_L = 75 pF. PCLK also has 750Ω pull-up resistor.

11/ t_4 refers to any allowable CLK period.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall verify the functional operation of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

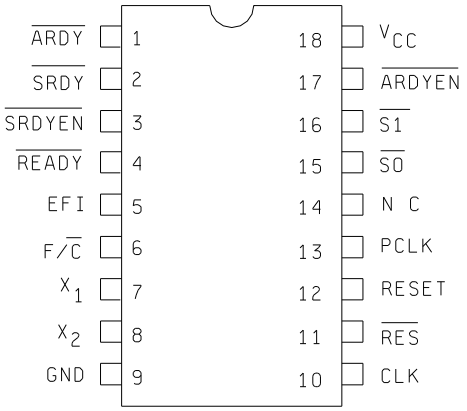


FIGURE 1. Terminal connections.

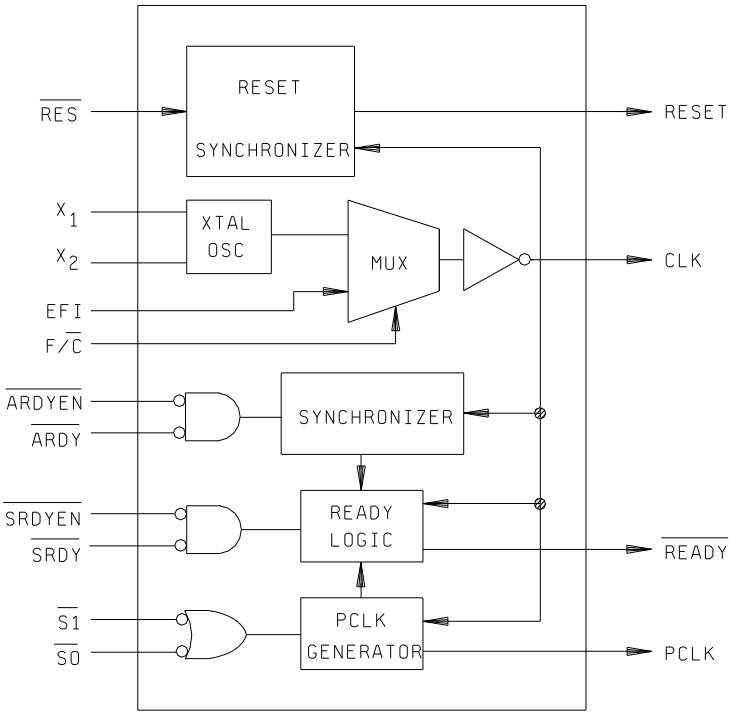


FIGURE 2. Logic diagram.

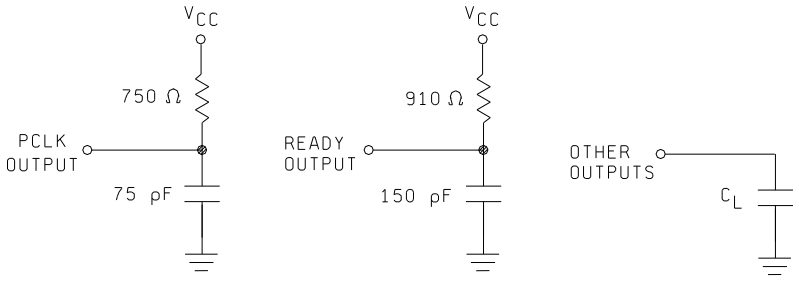
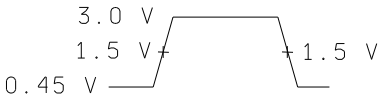
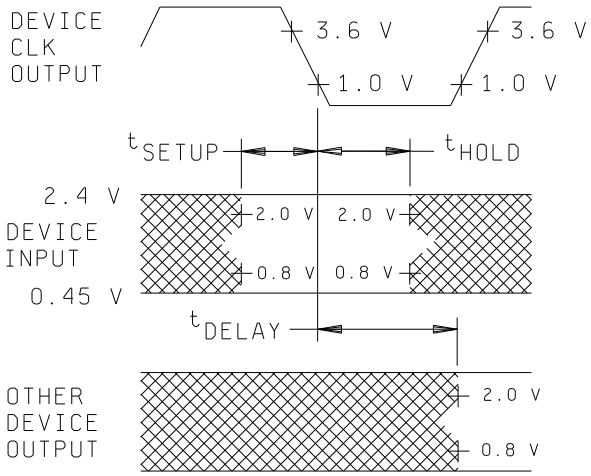


FIGURE 3. Output load.



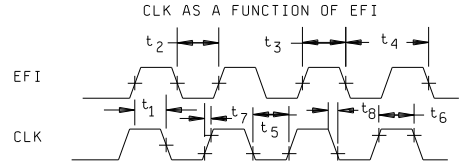
RESET, EFI DRIVE AND MEASUREMENTS POINTS

CLK OUTPUT MEASUREMENT POINTS



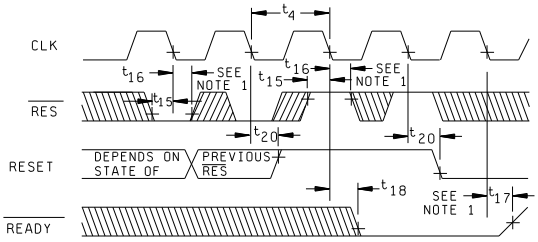
AC SETUP, HOLD AND DELAY TIME MEASUREMENT

FIGURE 4. Switching waveforms.

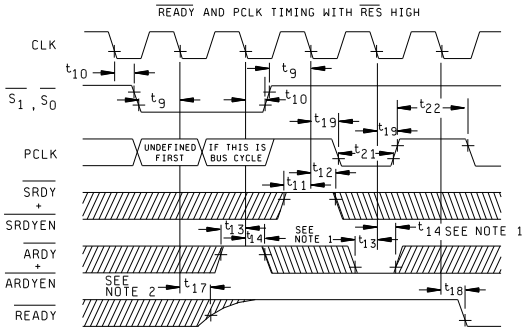


NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

RESET and $\overline{\text{READY}}$ timing as a function of $\overline{\text{RES}}$ with $\overline{\text{S1}}$ and $\overline{\text{S0}}$ HIGH



NOTES:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. Tie 910Ω ±5 percent pull-up resistor to the READY output.



NOTES:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. Tie 910Ω ±5 percent pull-up resistor to the READY output.

FIGURE 4. Switching waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical electrical parameters (method 5005)	2, 8a, 10

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECT, telephone (513) 296-6023.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-05-14

Approved sources of supply for SMD 5962-87734 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8773401VX	34649	MD82C284-10/B
5962-8773402VX	34649	MD82C284-8/B
5962-8773403VX	34649	MD82C284-6/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 West Chandler Boulevard Chandler, AZ 85226